

## REMARKS

### Status of the Application

Claims 1-5 are pending. Claims 1, 3, 4, 5 were rejected under 35 USC 103(a) as being unpatentable over Shiragaki (US Publication No. 2002/0162045) in view of Pierson Jr. (US 6,633,566). Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Shiragaki in view of Pierson Jr. as applied to claim 1, and further in view of Conoscenti et al. (US 5,627,836).

Applicant has amended claim 1 to more clearly define the invention. New claim 6 has been added. No new matter adds through the amendments. Entry and favorable consideration of the amendments and the RCE is requested.

### Claim Rejections- 35 U.S.C. 103(a)

Claims 1, 3, 4, 5 were rejected under 35 USC 103(a) as being unpatentable over Shiragaki (US Publication No. 2002/0162045) in view of Pierson Jr. (US 6,633,566).

Applicants respectfully traverse the rejections for reasons discussed below.

Claim 1 as amended recites:

“after low layer processing module detecting high layer processing module encountering the trouble, **the low layer transmission passage between the low layer processing module and the high layer processing module is broken, and the low layer processing module connects the broken passage to set up a bypass, so as to isolate the high layer processing module encountering a trouble.**

Shiragaki at least does not teach or suggest the above emphasized features of claim 1. First, as recited in claim 1, the trouble or failure occurs in the high layer processing module in the present invention, while Shiragaki does not teach that the failure occurs in layer A or layer B. Instead, layer A or B is used to recover the failure. If layer A or layer B itself failures, it cannot be used to recover the failure. Secondly, in the present invention, after low layer processing module detecting high layer processing module encountering the trouble/failure, the transmission passage between the low layer processing module and the high layer processing module is broken, and the low layer processing module connects the broken passage to set up a bypass, so as to isolate the high layer processing module encountering a trouble. Shiragaki clearly fails to

teach breaking the communication passage between layer A and layer B after detecting the failure. Instead, if layer A detects the failure, it will inform layer B and, after receiving the message from layer A, layer B will send A an authorization. Clearly, the passage between layer A and B is not broken.

Pierson clearly cannot cure the above discussed deficiencies of Shiragaki.

For the reasons discussed above, claim 1 is patentable over Shiragaki and Pierson. Claims 3-5 depend from claim 1 and, thus, are also patentable over Shiragaki and Pierson for at least the same reasons.

Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Shiragaki in view of Pierson Jr. as applied to claim 1, and further in view of Conoscenti et al. (US 5,627,836).

The Conoscenti was cited to teach that “a transparent virtual path connection is set up for the service passing the high layer processing module of the said node, namely for ATM, a cross connection, which changes neither virtual path identification nor virtual channel identification, will be set up, to avoid changing the service between upstream node and downstream node after passing high layer processing module of the said node” as recited in claim 2.

However, Conoscenti cannot cure the deficiencies of Shiragaki and Pierson as discussed in connection with claim 1. Therefore, claim 1 is patentable over Shiragaki, Pierson, and Conoscenti. Claim 2 depends on claim 1 and, thus, is also patentable over Shiragaki, Pierson, and Conoscenti for at least the same reasons discussed above.

Further more, Conoscenti does not specifically teach the above features recited in claim 2 as discussed in the previous response.

### **Conclusion**

In view of the foregoing amendments and remarks, it is respectfully submitted that claims 1-5 are patentable over the cited references. Allowance of this application is earnestly solicited.

The office is authorized to charge the RCE fee and three-month time extension fee and any other required fees in connection with the filing of this RCE to deposit account No. 500710.

Respectively submitted  
J.C. PATENTS

Date: November 5, 2009

/JIAWEI HUANG/  
Jiawei Huang  
Registration No. 43,330

4 Venture, Suite 250  
Irvine, CA 92618  
Tel.: (949) 660-0761